INTERNATIONAL JOURNAL OF RESEARCH IN TECHNOLOGY AND MANAGEMENT (IJRTM)
ISSN 2454-6240
www.ijrtm.com

PERFORMANCE ANALYSIS OF BCD ADDER ON FPGA

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ABSTRACT—Decimal adders and multipliers are the basic building block for arithmetic and logical unit and barrel shifters in today's high end processors and controllers. There are different levels of abstraction at which the power can be minimize. In this work an efficient BCD ADDER is analyzed in terms of power consumption by scaling the various parameters like voltage, frequency and load capacitance. The proposed designs are hardened and implement by means of VHDL and Xilinx ISE (integrated Software Environment) 12.2 and validated using Power targeting Vertex FPGA. Power consumption is discussed in terms of clock, signals, logic, input/ outputs and leakage.

Keywords—BCD Adder, Low Power, Scaling, VHDL, Xilinx

I. INTRODUCTION

Addition is utilized as a vital operation for processing the majority of the arithmetic functions, so it requires specific consideration. In digital electronics the term adder means a circuit which performs addition operation on numbers .ALU is the most important part of central processing unit where different mathematical and logical operations takes place. For addition binary numbers are used by digital adders normally. However, representation like BCD is also used to design an adder

There is a advantage of using BCD representation instead of binary representation, it is easy to covert string of a decimal number into the string of BCD representation. This quality is useful when we use fractional values because many values which are common, between zero and one cannot be represented by fixed and floating point binary representation. Therefore, BCD operation is efficient when BCD device is used. After reading the value from BCD device, a simple arithmetic operation is performed and then this BCD value is written to some other device. Software which are based on the decimal arithmetic cannot meet the required performance because of widespread range of decimal arithmetic.

Reviewing a number of literatures, it is found that for minimizing computational time, several ideas are proposed. Most of the modifications are done to minimize the computation time of carry, due to which proportionality constant may decrease. Though the addition operation in decimal representation consumes same time for propagation of carry as in binary representation, practical implementation saves the time as well as interfaces of coding. For designing high speed decimal adder, many techniques are being used. One of the techniques is to produce decimal sum directly. Decimal carries are produced through refinement of carry look ahead in second method. These two techniques is used to design a unit which process decimal arithmetic parallel.

The speed of computation of BCD adder is given most importance in many papers. The BCD algorithm for addition is suggested to have several enhancements by many designers. Some of the examples are direct decimal addition [3], decimal speculative addition [1,2], and conditional speculative decimal addition. But this enhancement in feasible speed can only occur when hardware is increased which results in high power consumption, which goes on rising because of the development in VLSI Technology. Besides speed, enhancement in performance of the adder also increases the consumption of power for which a suitable packaging needs to be build and also cooling techniques are to be there which sends out the heat from the processor[5]. But these additional facilities lead to increased cost. There are a number of algorithms and architecture which are proposed for BCD addition. But less focus is given to the issue above.

In this work the goal is to achieve an efficient BCD ADDER in terms of power consumption. This is observed by scaling various parameters like voltage, frequency and load capacitance.

II. OVERVIEW OF BCD ADDITION

Each digit is represented by its binary sequence in BCD coding. For encoding decimal number BCD is used. In BCD, conversion to digits is easy and it helps in faster calculation. When the addition of two decimal digits in BCD takes place with the carry generated from the previous least significant pair of digits, assuming the maximum value for input digits viz, 9+9+1 would result in 19. Equivalent sum in binary form will be in the range of 0 to 19 represented as 0000 to 10011 and equivalent sum in BCD will be in range of 0000 to 1 1001. When binary sum equals to or less than the 1001, the corresponding BCD digit is correct, but it results in invalid BCD digit when binary sum exceeds 1001. For correcting the digit, 6(0110)2 is added to the binary sum.

III. TECHNIQUES FOR LOW POWER

In this paper the major strategy involved for reducing power consumption of the BCD ADDER are described in the following sections-changes are done at the system level (simplification of algorithm) firstly. Scaling of parameters is performed, on which the power is dependent secondly.

3.1 Simplification of Algorithm

In general, to reduce the number of operations which are to be performed is a first-order goal, although in some situations, re-computation of an intermediate result may be cheaper than spilling to and reloading from memory. Optimizing compilers use technique, like strength reduction, common sub expression elimination, and optimizations for minimizing memory traffic are also useful in most circumstances in reducing power. Two methods are used to reduce power consumption and are implemented on the BCD ADDER

3.1.1 Coding Technique

For low power two methods are discussed. To use synthesis attributes for controlling the use of control signals at the signal or module level for low power design firstly. Second is coding-behavioral HDL or dataflow HDL. The BCD ADDER is programmed using all the possible combinations for the two four-bit inputs with a carry. The truth table for all output logic functions is constructed for all possible combinations of the inputs. The number of possible combinations is $2^9 = 512$ because the inputs are nine bits. Some of these combinations are invalid because a decimal digit is less than $(10)_{10}$ whereas, 4-bit number can take any value from 0 to $(15)_{10}$. The output is set to don't care when the input is invalid. This will help to minimize the output logic functions more.

3.1.2 Clock Gating

To turn off the inactive parts temporarily is one of the simplest ideas implemented in reduction of dynamic power is or put unused modules in standby mode. The technique applied is simple, to use Clock Enable. Clock gating may be applied at the function unit level for controlling switching activity by inhibiting input updates to function units whose outputs are not required for a given operation. By applying clock gating, entire subsystems may be gated off in the distribution network.

3.2 Scaling Of Parameters

Power is linearly dependent on the clock frequency and supply voltage. It also depends on the load capacitance. The scaling of parameters shows a change in the power consumption of the design.

3.2.1 Frequency Scaling

Performance of the adder can also be affected by frequency scaling but this can be dealt with parallelism technique. The junction temperature exceeds the maximum value of 85 ^{o}C at a very high frequency. For reducing the junction temperature, cooling aspects of the system (like increasing air flow) is improved. These parameters are kept constant for this scaling technique- Airflow is 250 LFM, Voltage is 1V & Capacitance is 5Pf.

3.2.2 Voltage Scaling

The performance of the adder can be affected by voltage scaling sometimes. Pipelining can be introduced for getting the same throughput in performance. These parameters are kept constant for this scaling technique- Frequency is 100MHz, Capacitance is 5pF, and Airflow is 250LFM

IV. RESULTS AND DISCUSSIONS

The comparison of power of BCD adder with and without clock gating is shown in Table 1. It is observed that reduction in power consumption takes place with clock gating. By temporarily disabling the clock signal on registers whose outputs does not affect outputs of circuit, clock and logic signal power are saved. Now, for further observations the BCD adder with clock gating is used .

Table 1: Power Comparison Analysis With CE and Without CE

ON-CHIP	WITHOUT CE (W)	WITH CE (W)
CLOCKS	0.019	0.007
LOGIC	0.003	0.000
SIGNALS	0.008	0.002
DCMs	0.000	0.000
IOs	0.074	0.008
LEAKAGE	0.329	0.328
TOTAL	**0.433**	**0.345**
JUNCTION TEMP.	**53.6**	**52.8**

From table 2, it is observed that power consumption increases with increase in value of capacitance and frequency, as their value linearly dependent on power consumption. On the other hand considerable rise in power takes place when voltage increases as it depends on power qudratically. Junction temperature's grey value shows that its value increased more than the maximum value (85^{o}C). Airflow is used for reducing the temperature. Hence, the parameters should be kept as minimum as possible for the low power.

Table 2: Scaling Of Parameters

	CAPACITANCE			FREQUENCY			VOLTAGE		
ON-CHIP(W)	5pF	15pF	25pF	100Mhz	10000Mhz	1Ghz	1 V	1.150V	1.200V
CLOCKS	0.007	0.007	0.007	0.007	0.013	0.641	0.007	0.008	0.008
LOGIC	0.000	0.000	0.000	0.000	0.017	0.019	0.000	0.000	0.000
IOs	0.002	0.002	0.002	0.002	0.047	3.700	0.002	0.002	0.002
SIGNALS	0.008	0.011	0.014	0.008	0.036	2.392	0.008	0.008	0.008
LEAKAGE	0.328	0.328	0.328	0.328	0.330	0.422	0.328	0.408	0.440
TOTAL POWER	**0.345**	0.348	0.351	**0.345**	0.443	7.174	**0.345**	0.426	0.458
JUNCTION TEMPERATURE (C)	**52.8**	52.9	52.9	**52.8**	53.6	109.5	**52.8**	53.5	53.8

V. CONCLUSION

In this paper different techniques to reduce power consumption in BCD adder is adopted. Extensive comparison regarding different values for the parameters (capacitance, frequency, voltage) is made.

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(2.11) $S_0=B_0$