COMPARATIVE ANALYSIS OF 4-BIT AND 8-BIT REVERSIBLE ARITHMETIC LOGIC UNIT (RALU) BASED ON REVERSIBLE GATE

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Abstract— With the advent of nanotechnology, transistors are getting smaller and growing in number according to Moore's Law. Reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. Reversibility plays an important role when energy efficient computations are considered. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. This paper comparative study is reversible design for 4-bit, 8-bit ALU. These ALU consists of different types of operations i.e. arithmetic and logical operations. The arithmetic operations include addition, subtraction, multiplication, division and the logical operations include NAND, AND, OR, NOT, XNOR, NOR and XOR. All the modules are being designed using the basic reversible gates. Simulation and verification of the design will perform using Xilinx 14.1i with different device family. In this paper, we have considered an 4-bit and 8-bit arithmetic logic unit (ALU) for implementation using RL gates and analyzed its performance for power dissipation and propagation delay.

Keywords—Component, formatting, style, styling, insert

I. INTRODUCTION

The technological advancements have made integration of billions of transistors on single die possible which has given the designers, the flexibility and freedom of putting more and more functionality on the same die. With this, the issue of heat dissipation is becoming of greater concern to researchers as the transistor heat dissipation reaches the Landauer limit. Reversible logic is predicted to be an alternative to conventional computing due to lesser energy dissipation and exponentially faster problem-solving capacity This has resulted in increased power consumption and has opened plethora of techniques dealing with it. Power dissipation in the electronic system is a very crucial limiting factor that can be reduced or minimized with the help of using reversible logic (RL) circuits. RL is emerging as an important research area in the recent years due to its ability to reduce the power dissipation, which is the main requirement in low-power digital system design. Energy dissipation is proportional to the number of bits lost during computation. The reversible circuits do not lose information bits and can generate unique outputs from specified inputs and vice versa. In modern very large scale integration (VLSI) systems, the power dissipation is high due to rapid switching of internal signals. Also, the systems designed using conventional circuits dissipate heat due to the loss of information bits during computation. Landauer [1] showed that the loss of every bit of information results in dissipation of KT*ln2 J of heat energy, where K is Boltzmann constant and T is temperature at which the operation is performed. Bennett [2] showed that the heat dissipation due to loss of information bits can be avoided

when the circuit is designed using RL circuits. A gate is considered reversible only if every input has a unique output assignment. Hence, there is a one-to-one mapping between the input and output vectors, i.e., it has same number of inputs and outputs [2]–[4]. The RL structures can be realized in the quantum logic system with minimum number of cells [5]. The complexity analysis of the ancilla bits can also be made with shortest path formulation and integer linear program (ming) (ILP) formulation for the RL [6]. An implementation of adder/subtractor and multiplier circuits using RL gates was done and its performance was analyzed. The paper is organized as follows: In Section 2, basic RL gates and their function are discussed. The various elements of ALU using the reversible gates are presented in Section 3. The simulated results of the various components of ALU are discussed in Section 4. In Section 5, performance of the various blocks is compared with the existing ones. Finally, conclusions are given in Section 6

II. REVERSIBLE GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. ALU stands for "Arithmetic Logic Unit." An ALU is an integrated circuit within a CPU or GPU that performs arithmetic and logic operations. Arithmetic instructions include addition, subtraction, and shifting operations, while logic instructions include Boolean comparisons, such as AND, OR, XOR, and NOT operations.

Definition 1: A reversible gate is a n x n circuit (n inputs, n s outputs) which uniquely maps each of its input to its corresponding output [3]. So, a reversible gate must satisfy the following conditions-

1) It should have equal number of inputs and outputs.
2) It should have one to one mapping between its inputs and outputs.

3) There should be neither feedback nor fanout in case of a reversible gate.

The above conditions ensure that the circuit designed using reversible gates does not lose any information bits as the inputs are processed by it and thus, the circuit is reversible. Such a circuit can overcome the energy efficiency barrier imposed by Landauer [1]. Maintaining the Integrity of the Specifications.

Definition 2: Ancilla inputs of a reversible gate are the inputs which should be maintained constant at either logic '0' or logic '1' so that the gate realizes the required Boolean function[3].

Definition 3: Garbage outputs of a reversible gate are the extra outputs which are of no logical use and are present only to maintain reversibility [3].

Reversible gates are bijective. There exist many reversible gates in the literatures [3], [4], [8], [9]. Among them 2*2 Feynman gate [8], 3*3 Fredkin gate [3], 3*3 Toffoli gate (TG) [4], 3*3 Peres gate (PG) [9], new gate (NG) [10] and 4*4 HNG gate [11] are the gates utilized to construct the reversible applications.
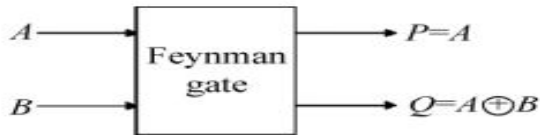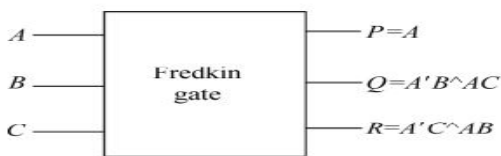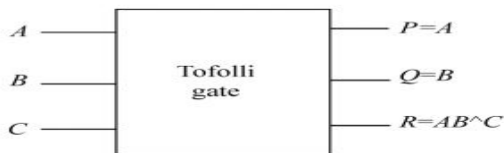

Figure 1. Feynman gate.

Figure 2. Fredkin gate.

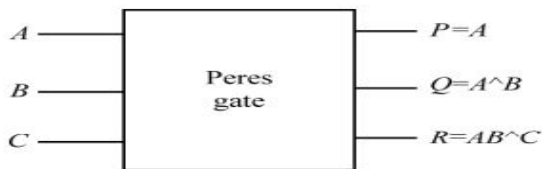

Figure 3. Tofolli gate.

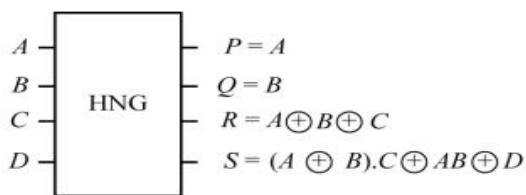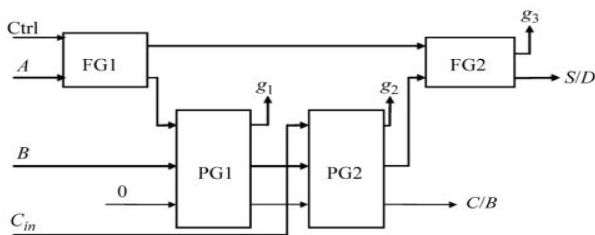Figure 4. Peres gate.

Figure 5. HNG gate.

Figure 6. Reversible design of full adder/subtractor.

III. LITERATURE SURVEY

The research on reversible logic is expanding towards both design and synthesis. Several researchers have been exploring techniques for synthesis of reversible logic circuits and many interesting contributions have been made. The synthesis of reversible circuits that employ a minimum number of gates and contain no redundant input output line-pairs (temporary storage channels) is investigated in; Researchers in have used the positive-polarity Reed-Muller expansion of a reversible function to synthesize the function as a network of Toffoli gates; The work in has illustrated the number of garbage outputs that must be added to a multiple output function to make it reversible [1].

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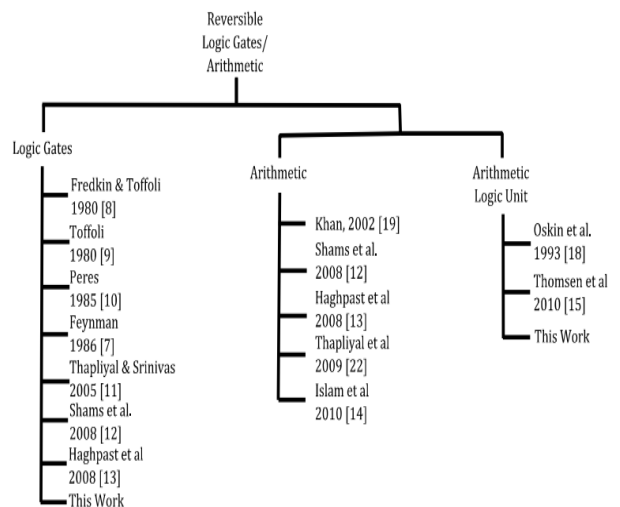

Figure7. Taxonomy of Relevant Works

Further a new reversible design method that uses the minimum number of garbage outputs is also proposed; the authors in investigate the problem of optimally synthesizing 4-bit reversible circuits using an enhanced bi-directional synthesis approach. Thus, in synthesis of reversible logic circuits, the optimization in terms of number of ancilla input bits and also the delay are not yet addressed except in the recent work which discusses about the post synthesis method for reducing the number of lines (qubits) in the reversible circuits [5].

The design of reversible sequential circuits was first introduced in 1988, in which the design of the JK latch was discussed. Later, the design of the RS latch was introduced

in. The design uses two cross-coupled reversible NOR gates as used in conventional logic for designing the RS latch. The design was clock less in nature, i.e., there was no enable signal. The NOR gates were designed from the reversible Fredkin gate. The work was limited to the design of RS latch only. In the authors introduced reversible latches such as D latch, T latch, etc., along with their corresponding flip-flops. The flip-flops were designed using master-slave strategy in which one reversible latch works as a master latch and the other works as a slave latch [6].
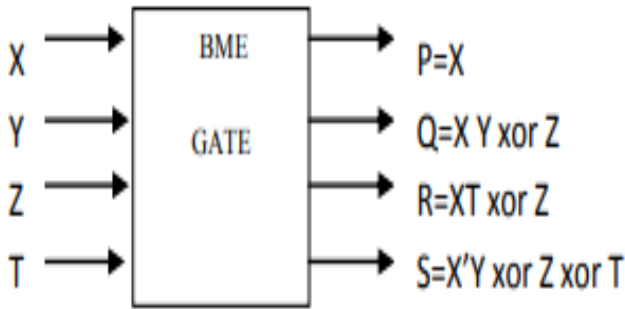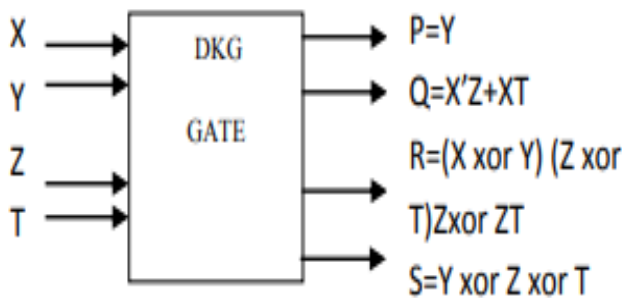

Figure 8. Block Diagram of BME Gate

Figure 9. Block Diagram of DKG Gate

The classical computational process which is irreversible, onebit of information is lost for each logical operation carried out by it. But in 1961, Rolf Landauer's principle states that for each bit of information. However, this loss of energy is legible for simple circuits and become significant for complex circuits. In 1973, Bennet showed that there would be no energy dissipation if computations are done in the reversible way [2]. Resultantly, a new paradigm in circuit design evolved with the aim of reducing the entropy increase and energy dissipation [3].

Table 1: Summary of Literature Review

Title	Methodology	Parameter	Scope
Design and Optimization of 8 bit ALU using Reversible Logic	Design 8-bit reversible ALU using COG and HNG Gate	Quantum cost = 26, garbage output = 9	Low power computing
Design and Implementation of Optimized 32-Bit Reversible Arithmetic Logic Unit	Design 32-bit reversible ALU using PFAG and HNG Gate	Quantum cost = 28, ancilla input = 12	CMOS technology
Design and Synthesis of Reversible Arithmetic and Logic Unit (ALU)	Design 16-bit reversible ALU using TSG and HNG Gate	Gate count =27 Delay = 12.64	Low area consumption
Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures	Design 4-bit reversible ALU using Toffoli and HNG Gate	Cost =24 Delay = 11	Less Complexity
Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors	Design 1-bit reversible ALU using Peres and HNG Gate	Number 17.4 ns	Low area and power
Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit	Design 8-bit reversible ALU using PFAG and HNG Gate	Quantum cost= 34, garbage output =14	Nano technology
Design and Analysis of 16 Bit Reversible ALU	Design 16-bit reversible ALU using HNG and PAOG Gate	Gate count ancilla input =12	Digital Circuit system
Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures	Design 1-bit reversible ALU using DPG and TOG Gate	Delay = 18.3 ns, slice =45, LUTs = 36	Digital Signal Processing

Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed according to the above constraints is known as a reversible logic device [4]. Reversibility becomes an essential parameter for the future computer designs [4]. Reversible gates or circuits allow the reconstruction of the inputs from the observed outputs. Reversible logic is applicable to the research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology [4]. A reversible circuit should be designed using minimum number of reversible logic gates.

Quantum technology is essentially reversible and is one of the important promising technologies for future computing systems. In addition to reversibility, it has unique features such as quantum superposition, quantum parallelism and quantum entanglement that allows for solving problems much more powerfully than in classical computing. (Observe that the quantum circuit is reversible when it calculates in Hilbert Space before the measurement. It is no longer reversible after measurement, since the probabilistic measurement cannot be reversed). Although only a few quantum algorithms are known in 2010, many problems can be reduced to some of these algorithms, for instance to the Quantum Fast Fourier Transform or to Grover's algorithm. Thus, any NP-hard problem can be reduced to Grover's algorithm to give a practically useful and substantial reduction in complexity for large values of N. This reduction is, however, not as high as in the case of the exponential speedup obtained by the famous Shor's quantum algorithm for integer factorization.

IV.   REVERSIBLE ADDER DESIGNS AND COMPARISON

A. Design of Reversible Ripple-Carry and Carry-Select Adders

In order to design the most efficient 32-bit reversible arithmetic logic unit, we designed and compared reversible implementation of ripple-carry, carry-select and carry look- ahead adders. A reversible ripple-carry adder and a reversible carry-select adder are designed using the new ALU. The ripple-carry adder has a cost of 40n-3 and a delay of 4n + 13. The most-significant bit of the ALU ties the Sum output to the SLT i/p of the least significant bit, and the SLT input for all other bits is 0. The reversible carry-select adder uses the carry out of the first n/2 bits as the control signal to a Fredkin gate implemented as a multiplexer, since the next n/2 bits are calculated with both a carry-in of 0 and a carry-in of 1, which requires a cost of 40(3n/2)-3 and a delay of 2n + 19.

B. Reversible Kogge-Stone Cumulate Logic

Next, a reversible carry look-ahead adder based on the Kogge-Stone adder is presented [9]. First, a RKS Cumulate utilized in the calculation of the carry out signal is designed and verified. The cost of the RKSC is 14 and it has a worst-case delay of 4. A cost and delay analysis of the presented adders in the ALU implementation is presented in Table 2.

The ripple-carry adder has the lowest cost, but the highest delay. The carry look-ahead adder has a prohibitively-high cost, but the most-desirable delay.

Table 2: Cost and delay comparison of 4-bit reversible adders.

	Ripple-Carry	Carry-Select	Kogge-Stone
Cost	192	293	2287
Delay	128	83	25

C. Comparison of Reversible Ripple-Carry and Carry-Select Adders with Sparsity

The Kogge-Stone adder may be enhanced to reduce overhead and design complexity by generating a carry every *n*-bits instead of every bit, and the carry is used for the carry- in of an n-bit ripple-carry or carry-select adder. The number *n* is defined as sparsity. This implementation was designed and tested for sparsity-4, 8 and 16 with the corresponding n- bit ripple-carry and carry-select adders. The cost and delay comparison of each implementation is shown in Table 5. The design for each adder presented in Table 5 was verified using VHDL in Xilinx 12.4.

Table 3 : Cost and delay comparison of modified carry look-ahead implementations for 8-bit reversible adders

	Sparsity-4	Sparsity-8	Sparsity-16
Ripple-Carry	Cost: 666 Delay: 40	Cost: 462 Delay: 56	Cost: 316 Delay: 88
Carry-Select	Cost: 802 Delay: 37	Cost: 578 Delay: 45	Cost: 422 Delay: 61

V. PROPOSED METHODOLOGY AND RESULT DISSCUSSION

The RALU utilizes the DKG gate and BME gate to produce eight logical calculations: transfer A, addition, Sub, XOR, OR, AND, NOT and NAND. The cost and delay calculations are identical to the ALU in figure 10. The RALU has 8 inputs and 8 outputs. The inputs consist of three data inputs (A, B and Cin) and five (S0, S1, S2, S3, S4) lines.
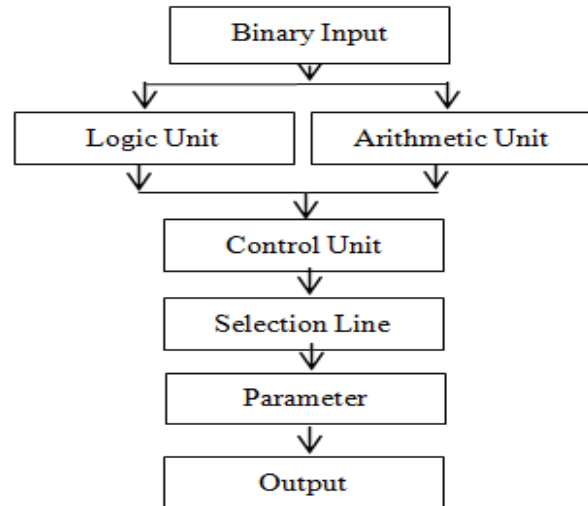

Figure 10: Flow of bit Slice ALU

The proposed implementation is programmed (Described) and implemented using VHDL language which is a Hardware Description Language that was developed by the Institute of Electrical and Electronic Engineers (IEEE) as a standard language for describing the structure and behavior of digital electronic systems. It has many features appropriate for describing the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips. The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

1. Design 4-bit and 8-bit using different types of reversible gate.
2. Design different types of programmable reversible gate and compared.
3. Design free garbage based architecture using different types of input and compared existing algorithm. Hand calculation of delay and area in reversible arithmetic logic unit in different inputs. All the modules design to different device family i.e. Spartan-3, Virtex-4 and Virtex-7.

VI. CONCLUSION

The 4-bit reversible ALU is designed by integrating various sub modules that includes adder/subtract or, and logical unit. The logical unit performs AND, OR, NOR, XOR, NAND. The performance evaluation of the various sub modules are carried out using Modalism 6.5 tools and it was found that the circuits designed using reversible logic showed reduced delay and power. As a future work more arithmetic and logical function can be used.

RL circuit is an emerging technology with promising applications because of its low-power dissipation. In this paper, a novel architecture of a reversible 8-bit ALU has been proposed and it is implemented in circuit level. Each block of the ALU was designed using the basic reversible gates. The simulation and synthesized result shows that RL-based design dissipates less power up to maximum of 39% improvement and 10% improvement in the delay. Thus the reversible ALU structure is suitable for portable low-power applications. In future, this design can be extended to 16, 32 and 64 bits. A reversible divider can also be designed and included into this ALU. Moreover, this design may be extended to gate level implementation.

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